REMARKS

The Examiner's Office Action of May 18, 2005 has been received and its contents reviewed. Applicants would like to thank the Examiner for thorough review and consideration given to the above-identified application, and for indicating that claims 7 and 9 contain allowable subject matter and would be allowable if amended to overcome a 35 USC §112, 2nd paragraph rejection.

Claims 1-10 are still pending in the present application, of which claims 1, 7 and 9 are independent. By this amendment, claims 1, 3, 8 and 10 have been amended.

Referring now to the Office Action, the drawings stand objected to because Fig. 2 does not include reference to node "n21" and Fig. 3 does not include reference to nodes "n31" and "n32", as discussed in the specification. In response, Applicants submit herewith Replacement Sheets for Figs. 2 and 3.

The specification stands objected to as the Examiner alleges the title of the invention is not descriptive and the abstract of the disclosure should be directed to the level shifting circuit of the invention. In response, Applicants respectfully submit that the title is sufficiently indicative of the invention without being overly verbose. The Examiner's attention is respectfully directed to U.S. Patent No. 6,700,434, for example, which has the succinct title of "*Substrate Bias Voltage Generating Circuit*". The above-mentioned title of the invention of U.S. Patent No. 6,700,434 was deemed acceptable by the Examiner. Hence, the title of the invention of this instant application should also be acceptable. Further, an abstract of the disclosure, which appears on the front page of a patent reference and below the title of the invention, should provide more details of the invention, and a reader should not have to rely on the title to understand the details of the invention. However, should the Examiner still maintain this rejection, Applicants would consider amending the title of the invention.

The abstract of the disclosure stands objected to as the Examiner asserted that the abstract should concentrate on the level shift circuit of the invention. In response, Applicants have amended the abstract, as attached, to improve the description of the level shifting circuits, which are a part of the substrate voltage generating circuit of the invention.

The disclosure stands objected to as containing informalities. Applicants have amended the specification to correct the following:

With respect to page 3, line 20 to page 4, line 2 and page 16, lines 16-17 identifying Fig. 3 as a "substrate voltage generating circuit", Applicants have amended the specification, as shown above, to change the above-mentioned occurrences of "substrate voltage generating circuit" to "level shift circuit".

With respect to page 6, line 2, Applicants have amended "1.5V" to "-1.5V" to identify the substrate voltage V_{BB} is lower than power supply voltage V_{SS}.

With respect to the typographical error "sown" on page 8, lines 8 and 15, Applicants have amended "sown" to "shown".

With respect to the typographical error "NADN" on page 8, line 13 and page 9, line 2, applicants have corrected the errors to "NAND".

With respect to the Examiner's question "where does VBB come from" and "how VBB is transferred out of OUT.vbb when switch element SW1 is on", and with respect to the Examiner's assertion that VBB is VSS at the output node OUT.vbb because n1 and n2 are directly coupled to VSS, Applicants respectfully submit that one of ordinary skill in the art would understand that c1 at node n1 and c2 at node n2, as well as VSS, affect voltage VBB at the output node OUT.vbb. Hence, it would be erroneous to conclude that VBB is VSS at the output node OUT.vbb because n1 and n2 are directly coupled to VSS as contended by the Examiner.

With respect to the reference to nodes "n31" on page 17, lines 11-12, Applicants have corrected node "n31" to node "n32". With respect to node "n32" on page 18, line 2, Applicants have changed "n31" to "n32". These amendments are consistent with the drawing amendment submitted above with respect to Fig. 3. As shown in corrected Fig. 3, nodes "n32" and "n31" are now shown in Fig. 3. Node "n32" is located between the drain of PMOS P32 and the drain of NMOS N32, and node "n31" is located between the drain of PMOS P31 and the drain of NMOS N31.

With respect to page 17, line 9, referring to the source of PMOS P32 as connected to the "second power supply node to which the power supply voltage VDD is supplied", Applicants have amended the specification, as shown above, to change "second" to "first", as the Examiner correctly pointed out that VDD is a voltage of the first power supply.

With respect to the double definite article "the the" on page 19, line 17, Applicants have deleted the second occurrence of "the".

In addition to correcting all informalities noted by the Examiner, Applicants have also amended page 12, lines 7-8 to change "substrate voltage VBB" to "power supply voltage VSS" to correct an obvious inadvertent error. Note that Fig. 1 shows the output of NAND 1 can only have a voltage level of VDD or VSS (i.e., High or Low) into in.101 input of the level shift circuit 101.

Claims 1-6 stand rejected under 35 U.S.C. §112, first paragraph, as the Examiner alleged that, while the specification is enabling for level shift circuit, it does not reasonably provide enablement for a substrate voltage generating circuit. The Examiner asserted that although Fig. 1 shows a substrate voltage generating circuit that generates substrate voltage VBB at its output terminal, the figure and disclosure do not clearly show/disclose how this is actually accomplished. In response, Applicants respectfully submit the following remarks:

First, there are typographical errors in the specification that have been corrected as discussed above. With these errors in the original specification and drawings, the explanation of the operation and structure of the substrate voltage generating circuit of the present invention may be may be confusing and difficult to understand. However, having amended the specification and drawings, as discussed above, the errors are now corrected and the specification should now be clearer in explaining how VBB is generated by the substrate voltage generating circuit.

Applicants note that the claimed invention as recited in claim 1 is not only directed to the level shift circuits 101 and 102 but also to the substrate voltage generating circuit that includes the level shift circuits 101 and 102 and other claimed limitations, such as the switch circuit. The specification clearly describes the level shift circuits 101 and 102 and their cooperation with other features that together with the level shift circuit make Applicants' claimed substrate voltage generating circuit to generate a substrate voltage VBB (i.e., V_{BB}).

At this juncture, Applicants respectfully invite the Examiner to study the description of how the presently claimed invention operates in generating VBB (i.e., V_{BB}) in reference to the first power supply voltage VDD (i.e., V_{DD}) and second power supply voltage VSS (i.e., V_{SS}). For example, beginning on page 11, line 8, the description of how the operation of the substrate voltage generating circuit according to a first embodiment, as shown in Figs. 1 and

2, is discussed. In another example, starting on page 18, line 13, the description of how the presently claimed invention according to a second embodiment, as shown in Figs. 1 and 3, is discussed.

As shown in Fig. 1, for example, the potential level inputs and outputs of each component are clearly shown. For example, NAND 1 can have either VDD or VSS as an output voltage level, output out.101 of level shift circuit 101 can have either VDD or VBB as an output voltage level, and so on. Hence, the behavior of each element in response to a certain input is clearly shown from the input signal OSC, /OSC and pump, power supply input VDD and VSS, to the final output signal OUT.vbb with substrate voltage VBB (i.e., V_{BB}).

Applicants note that the output substrate voltage VBB generated is also used as an input to the source of the 5th and 6th transistors N3 and N4, respectively, in Fig. 2. Also, VBB is used as an input voltage at the source of the 5th and 6th transistors N33 and N34, respectively, as shown in Fig. 3. This feedback of the generated VBB substrate voltage, although not explicitly described in the specification, is clearly shown in Fig. 1 with a connection of OUT.vbb to level shift circuits 101 and 102.

If the Examiner cannot follow the description in the amended specification detailing the operation of the claimed invention, and if the Examiner would like to go over the specification in detail, Applicants would request the Examiner to give Applicants an opportunity to conduct a personal interview with the Examiner.

As an alternative, Applicants would prepare an affidavit confirming that the disclosed substrate voltage generating circuit, which includes the level shift circuits, do operate as described and claimed, if the Examiner desires such an affidavit.

Applicants respectfully invite the Examiner to study the following example of U.S. patents, which relate to substrate voltage generators, if necessary, to gain additional background in this art:

U.S. Patent No.	Inventor
5,039,877	Chern,
5,838,189	Jeon,
5,905,582	Gans et al.,
6,198,341	Ryu,
6,259,310	Kawamura,
6,239,650	Tsay et al., and
6,316,985	Kobayashi.

Claims 1-10 stand rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner does not understand, in claim 1, lines 5-6, the "output node receiving a voltage having a third potential level". In response, Applicants have amended claim 1, as shown above, to delete "receiving a voltage".

Further, the Examiner deemed the limitations "first potential level", "second potential level", and "third potential level" as confusing. In response, Applicants note that it is clear from the specification that a first potential level is VDD, a second potential level is VSS, and a third potential level is VBB. VDD is clearly disclosed in the specification as a high (H) potential level, while VSS is a low (L) potential level, and VBB, which is the generated substrate voltage, has a potential that is lower than the second potential level VSS. The drawing figures clearly show, e.g, "VDD/VSS", "VDD/VBB", etc., which means that the output potential level is either VDD or VSS, or VDD or VBB, etc.

The Examiner asserted that claim 2, lines 6-7, are misleading with respect to the gate of the second transistor receiving the input signal because transistors P1/P2 receive complementary input signals as shown in Fig. 2. In response, Applicants respectfully direct the Examiner's attention to claim 1, particularly the following limitation:

"a level shift circuit which is coupled between the first power supply node and the output node, which receives an input signal having the first and second potential levels..."[emphasis added].

As recited in claim 2, the input signal is of a first and second potential. As supported by the specification and Fig. 1, the input signal is VDD or VSS (i.e., VDD/VSS). Hence, one of ordinary skill in the art would understand that VDD is complementary to VSS in this case. That is, while the gate of P1 receives VDD potential level as an input, the gate of P2 receives potential VSS as input signal. This explanation is also applicable to the Examiner's question relating to claims 3, 7 and 9 regarding the same alleged misleading language.

Further, Applicants note that INV 7, in Fig. 1, is an inverter which has an input of VDD/VSS and an inverted output amplitude of VDD/VSS, as disclosed on page 9, line 8. Thoughout the specification, it can be seen that VDD is "H" logic and VSS is "L" logic, such as on page 12, lines 4-5, for example.

The Examiner asserted that claims 3 and 9 are inconsistent with page 18, lines 4-8 of the specification, as claims 3 and 9 do not recite 5th and 6th transistors as having a thicker gate oxide film than that of the 3rd and 4th transistors. In response, Applicants have amended claims 3 and 9, as shown above, to specify that the thickness of the gate oxide film of the 3rd and 4th transistors is greater than the gate oxide film of the 5th and 6th transistors.

The Examiner rejected claims 8 and 10 as there is no proper antecedent basis for "the substrate voltage generating circuit". In response, Applicants have amended claims 8 and 10, as shown above, to overcome the rejection of these claims.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections and objections.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. However, if the Examiner deems that any issue remains after considering this response, he is invited to call the undersigned to expedite the prosecution and work out any such issue by telephone.

Respectfully submitted,

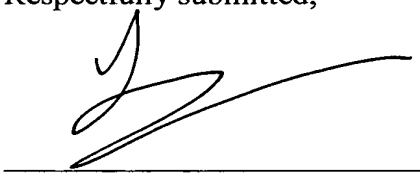

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FIG. 2

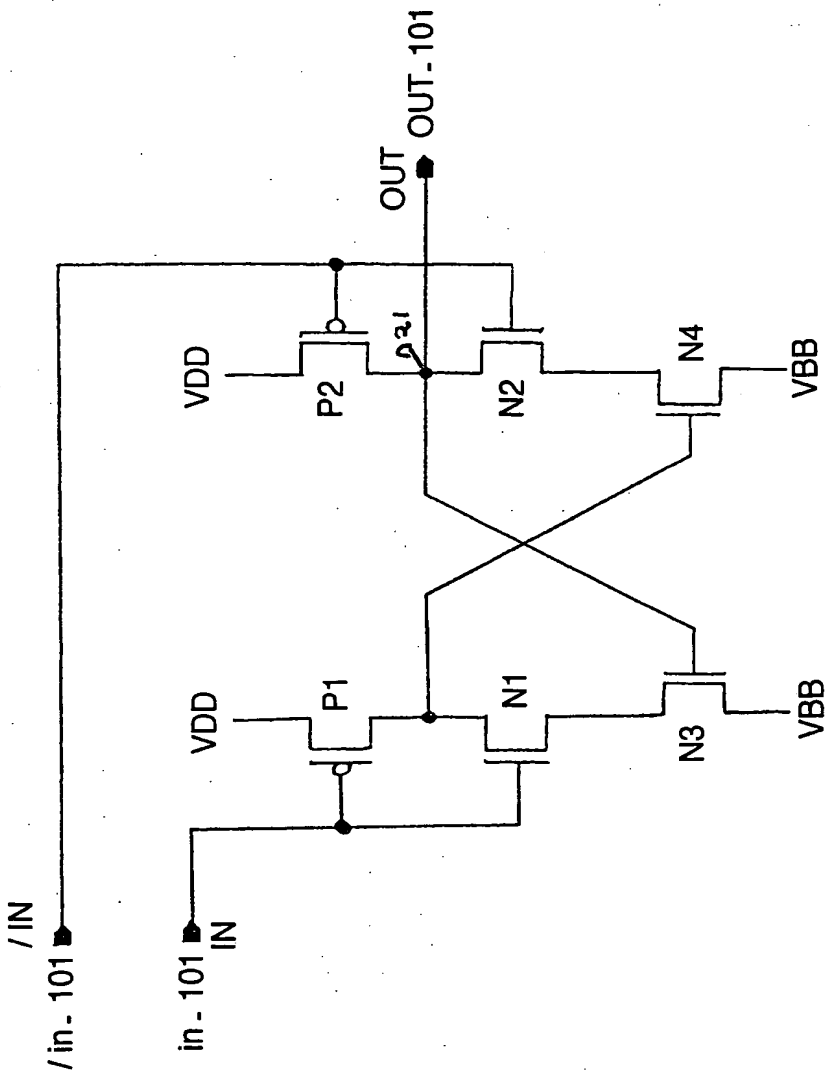
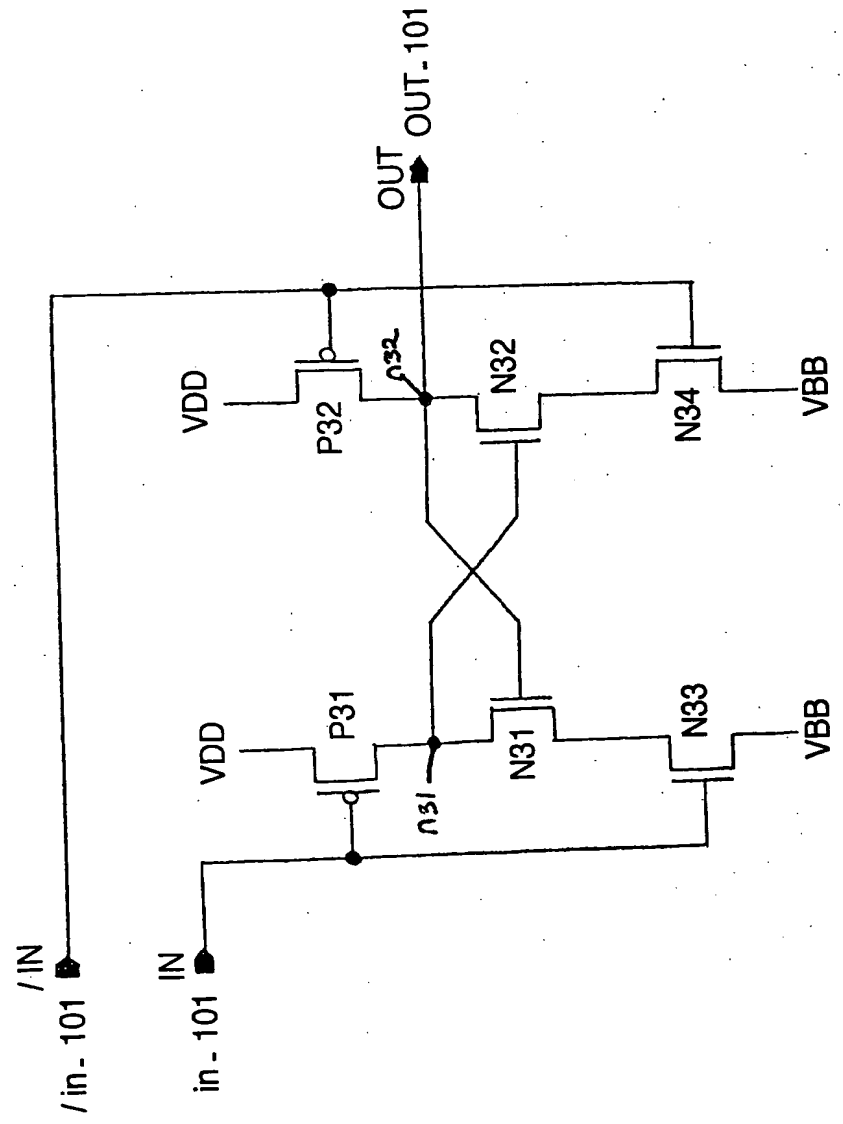


FIG. 3


OUT
OUT_101
VDD
P32
N32
N34
VBB
VDD
P31
N31
N33
VBB
/IN
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IN
in_101